

- Tentative Specification
- Preliminary Specification
- Approval Specification

**MODEL NO.: V400HJ2**

**SUFFIX: LE2**

Customer:	
APPROVED BY	SIGNATURE
<u>Name / Title</u> _____	
Note	
<hr/> Please return 1 copy for your confirmation with your signature and comments.	

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REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.0	Nov. 22, 2010	All	All	The approval specification was first issued.

## 1. GENERAL DESCRIPTION

### 1.1 OVERVIEW

V400HJ2-LE2 is a 40" TFT Liquid Crystal Display module with LED Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 16.7M colors (8-bit). The converter module for backlight is built-in.

### 1.2 FEATURES

- High brightness (450 nits)
- High contrast ratio (5000:1)
- Fast response time (Gray to gray average 9.0 ms)
- High color saturation (NTSC 72%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 60 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- RoHS compliance

### 1.3 APPLICATION

- Standard Living Room TVs
- Public Display Application
- Home Theater Application
- MFM Application

### 1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	885.6 (H) x 498.15 (V) (40" diagonal)	mm	(1)
Bezel Opening Area	891.7 (H) x 504.8 (V)	mm	
Driver Element	a-Si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.15375 (H) x 0.46125 (V)	mm	-
Pixel Arrangement	RGB Vertical Stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare Coating (Haze 11%)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. CMI reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	920.2	921.7	923.2	mm	(1)
	Vertical (V)	536.3	537.8	539.3	mm	(1)
	Depth (D)	20.5	22	23.5	mm	(2)
	Depth (D)	22.4	23.9	25.4	mm	(3)
Weight		-	6950	-	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth is between bezel to T-CON cover.

Note (3) Module Depth is between bezel to converter cover.

**2. ABSOLUTE MAXIMUM RATINGS**

**2.1 ABSOLUTE RATINGS OF ENVIRONMENT**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	°C	(1)
Operating Ambient Temperature	TOP	0	50	°C	(1), (2)
Shock (Non-Operating)	SNOP	—	50	G	(3), (5)
Vibration (Non-Operating)	VNOP	—	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

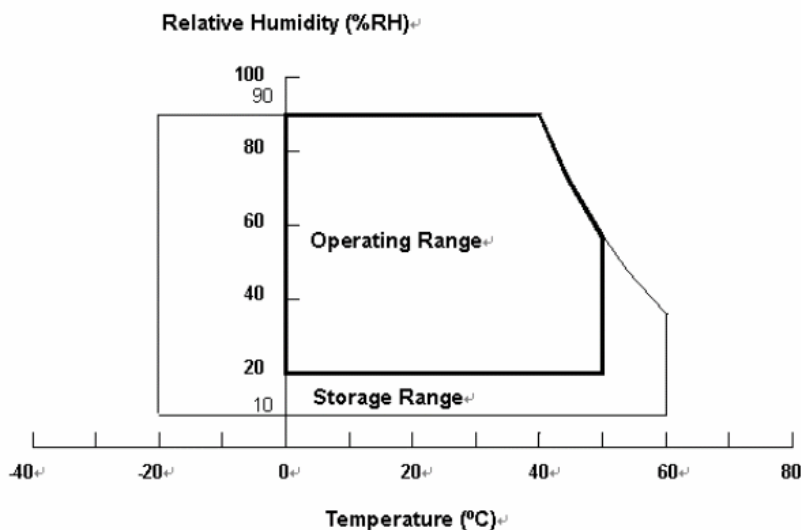
- (a) 90 %RH Max. ( $T_a \leq 40\text{ }^\circ\text{C}$ )
- (b) Wet-bulb temperature should be 39 °C Max. ( $T_a > 40\text{ }^\circ\text{C}$ )
- (c) No condensation

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



**2.2 PACKAGE STORAGE**

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 °C at normal humidity without condensation.
- (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

**2.3 ELECTRICAL ABSOLUTE RATINGS**

**2.3.1 TFT LCD MODULE**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

**2.3.2 BACKLIGHT CONVERTER UNIT**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Light Bar Voltage	VW	—	40.7	VRMS	
Converter Input Voltage	VBL	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and Internal PWM Control.



3. ELECTRICAL CHARACTERISTICS

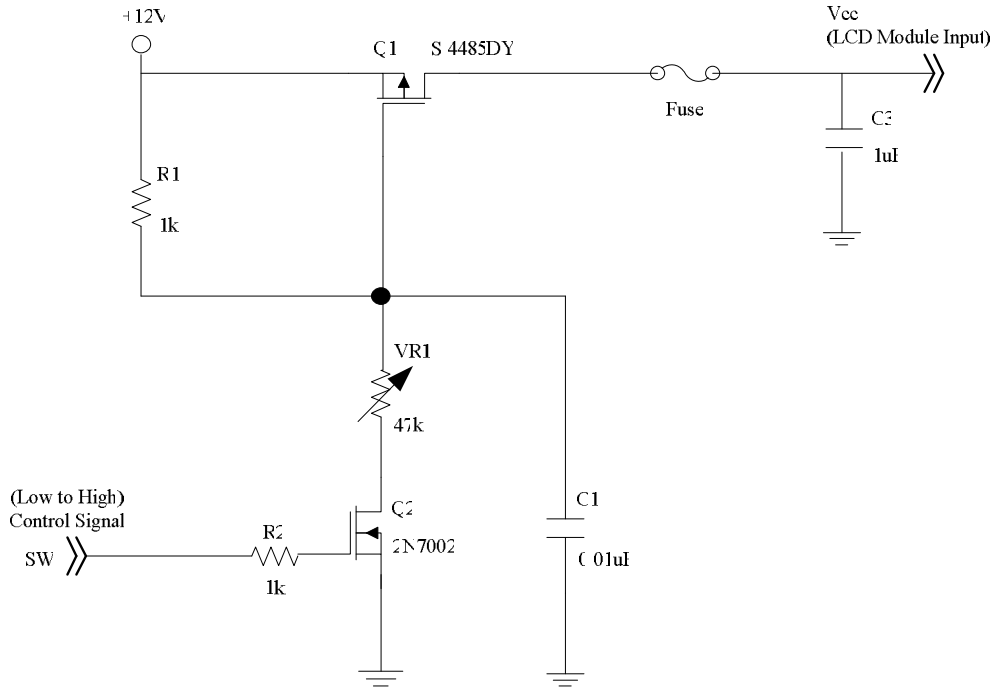
3.1 TFT LCD MODULE

(Ta = 25 ± 2 °C)

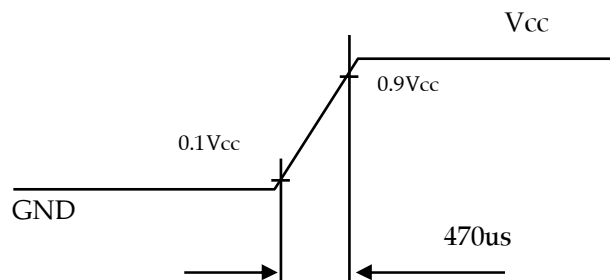
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V <sub>CC</sub>	10.8	12	13.2	V	(1)
Rush Current		I <sub>RUSH</sub>	—	—	3.6	A	(2)
Power Consumption	White Pattern	P <sub>T</sub>	—	4.6	5.5	W	(3)
	Black Pattern			4.3	5.2		
	Horizontal Pattern			6.7	8.2		
Power Supply Current	White Pattern	—	—	0.38	0.46	A	(3)
	Black Pattern	—	—	0.36	0.43		
	Horizontal Pattern	—	—	0.56	0.68		
LVDS interface	Differential Input High Threshold Voltage	V <sub>LVTH</sub>	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V <sub>LVTL</sub>	—	—	-100	mV	
	Common Input Voltage	V <sub>CM</sub>	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	V <sub>ID</sub>	200	—	600	mV	
	Terminating Resistor	R <sub>T</sub>	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	V <sub>IH</sub>	2.7	—	3.3	V	
	Input Low Threshold Voltage	V <sub>IL</sub>	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition :



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at  $V_{cc} = 12\text{ V}$ ,  $T_a = 25 \pm 2\text{ }^\circ\text{C}$ ,  $f_v = 60\text{ Hz}$ , whereas a power dissipation check pattern below is displayed.

a. White Pattern



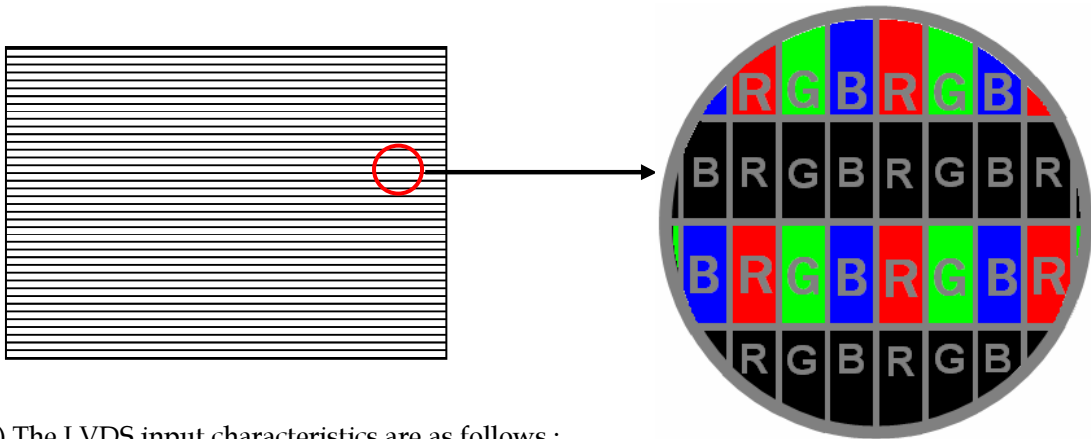
Active Area

b. Black Pattern

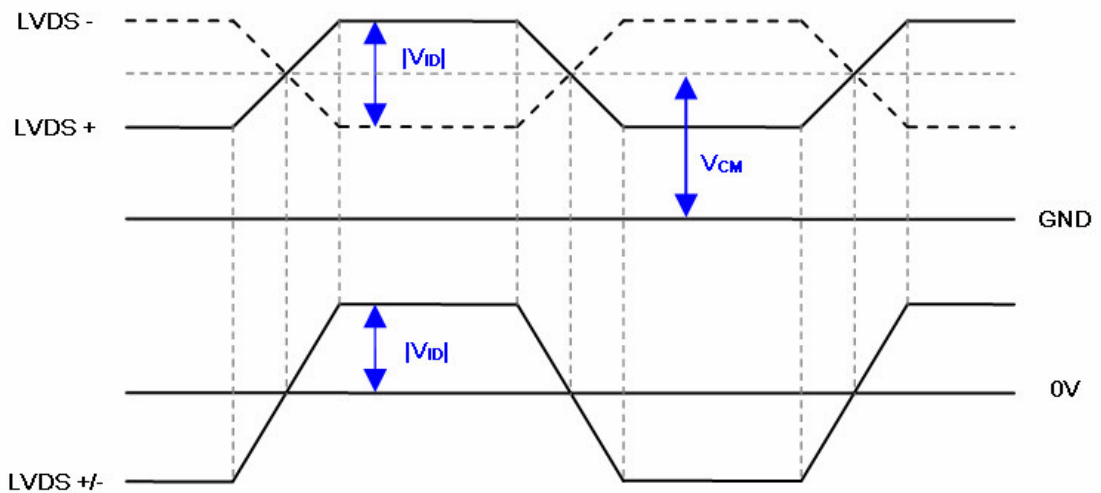


Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows :



### 3.2 BACKLIGHT CONNECTOR PIN CONFIGURATION

#### 3.2.1 LED LIGHT BAR CHARACTERISTICS

(Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Total Current (6 String)	If	—	720	763.2	mA	
One String Current	IL	—	120	127.2	mA	
LED Forward Voltage	V <sub>f</sub>	2.9	3.2	3.7	V <sub>DC</sub>	I <sub>L</sub> =120 mA
One String Voltage	V <sub>W</sub>	31.9	—	40.7	V <sub>DC</sub>	I <sub>L</sub> =120 mA
One String Voltage Variation	ΔV <sub>W</sub>	—	—	2	V	
Life time	—	30,000	—	—	Hrs	(1)

Note (1) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value, Operating condition: Continuous operating at Ta = 25±2°C, I<sub>L</sub> =120 mA

#### 3.2.2 CONVERTER SPECIFICATION

(Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P <sub>BL</sub>	—	57	66	W	(1),(2) I <sub>L</sub> = 120 mA
Converter Input Voltage	V <sub>BL</sub>	22.8	24	25.2	V <sub>DC</sub>	
Converter Input Current	I <sub>BL</sub>	—	2.375	2.75	A	Non Dimming
Input Inrush Current	—	—	—	3.7	A <sub>peak</sub>	V <sub>BL</sub> =24V, (I <sub>L</sub> =typ.) (3)
Dimming Frequency	F <sub>B</sub>	90	160	190	Hz	
Minimum Duty Ratio	D <sub>MIN</sub>	5	10	—	%	(4)

Note (1) The power supply capacity should be higher than the total converter power consumption PBL. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when converter dimming.

Note (2) The measurement condition of Max. value is based on 40" backlight unit under input voltage 24V, average LED current 120 mA and lighting 1 hour later.

Note (3) The duration of rush current is about 30ms.

Note (4) 5% minimum duty ratio is only valid for electrical operation.

3.2.3 CONVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note	
				Min.	Typ.	Max.			
On/Off Control Voltage	ON	V <sub>BLON</sub>	—	2.0	—	5.0	V		
	OFF		—	0	—	0.8	V		
External PWM Control Voltage	HI	V <sub>EPWM</sub>	—	2.0	—	5.25	V	Duty ON	(5)
	LO		—	0	—	0.8	V	Duty OFF	
Error Signal		ERR	—	—	—	—	V	Abnormal : Open Connector Normal : GND	(4)
VBL Rising Time		Tr1	—	30	—	—	ms	10%-90% V <sub>BL</sub>	
Control Signal Rising Time		Tr	—	—	—	100	ms		
Control Signal Falling Time		Tf	—	—	—	100	ms		
PWM Signal Rising Time		T <sub>PWMR</sub>	—	—	—	50	us		
PWM Signal Falling Time		T <sub>PWMF</sub>	—	—	—	50	us		
Input Impedance		R <sub>IN</sub>	—	1	—	—	MΩ		
PWM Delay Time		T <sub>PWM</sub>	—	100	—	—	ms		
BLON Delay Time		T <sub>on</sub>	—	300	—	—	ms		
BLON Off Time		T <sub>off</sub>	—	300	—	—	ms		

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in following figure. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

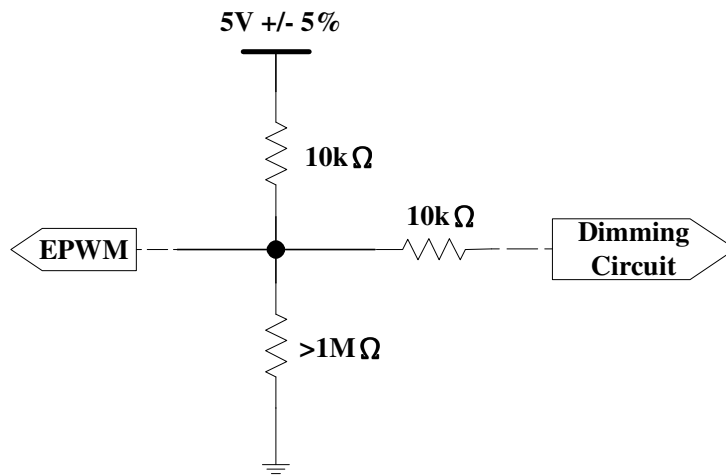
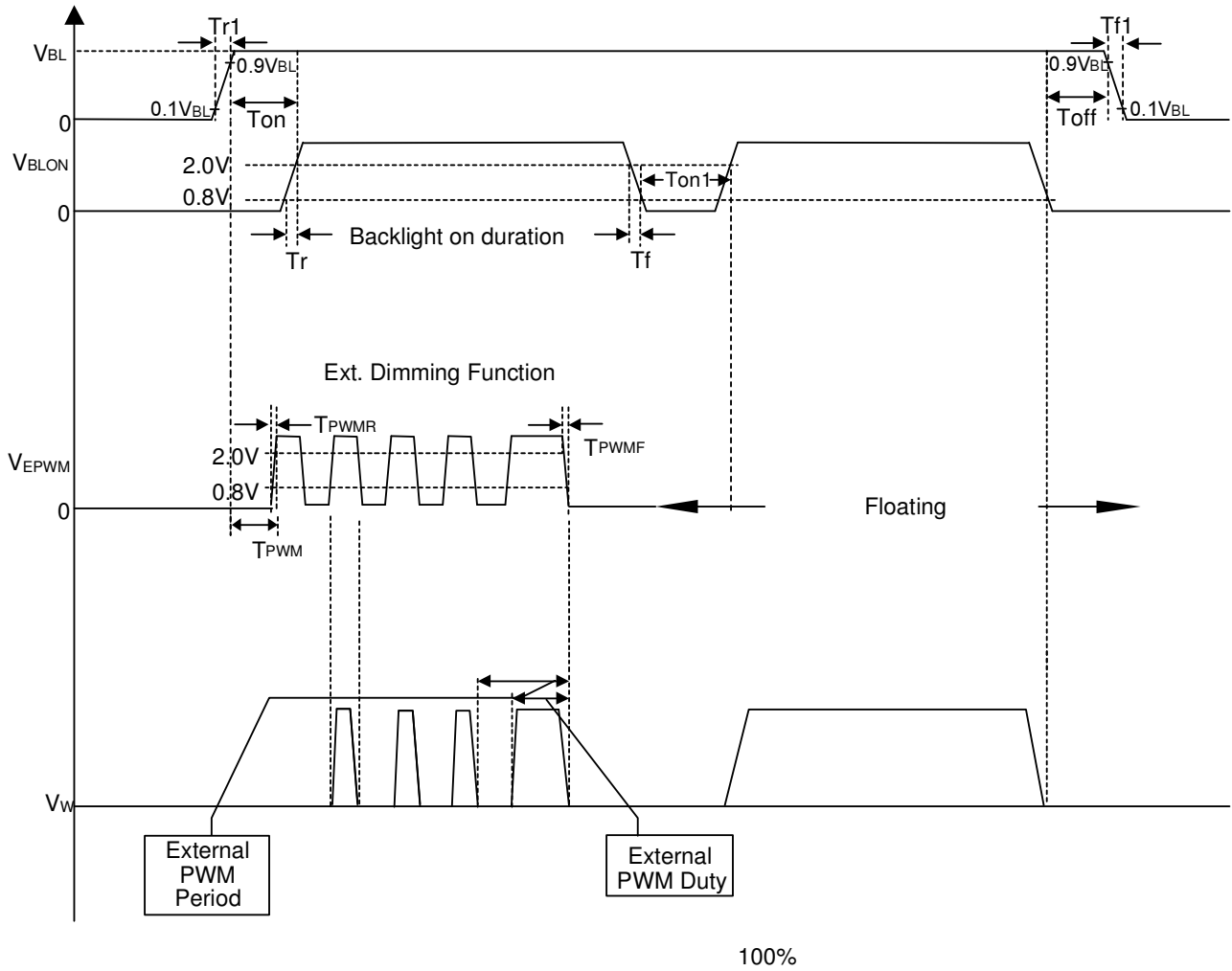
Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions :

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

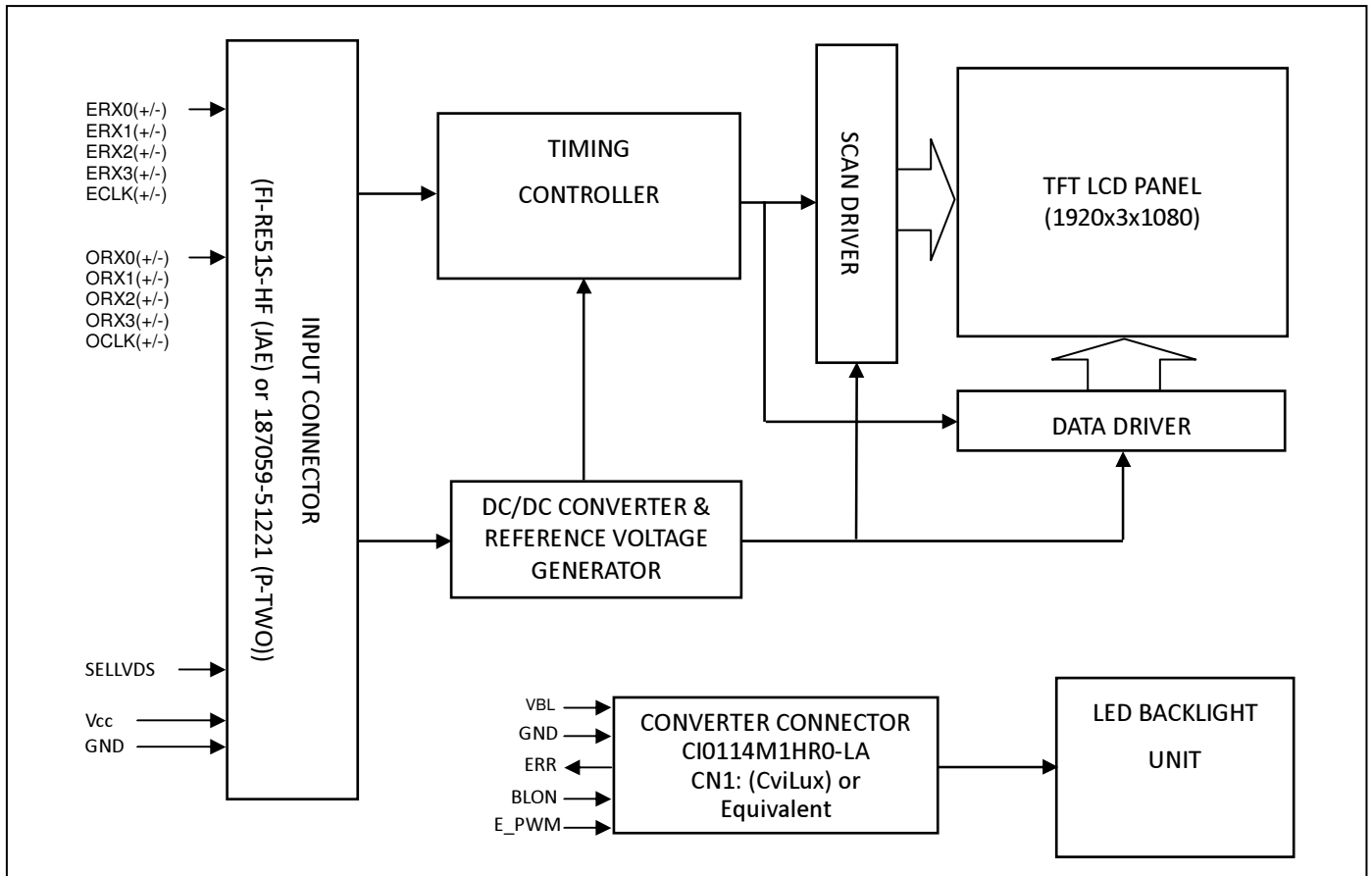
Note (4) When converter protective function is triggered, ERR will output open collector status.

Note (5) The EPWM interface that inserts a pull up resistor to 5V in Max Duty (100%), please refers following figure.



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE INPUT

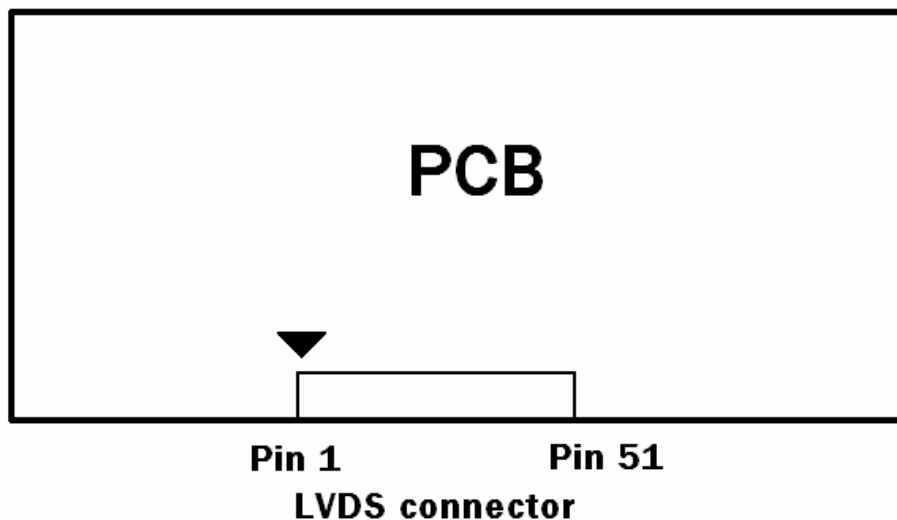
CNF1 Connector Pin Assignment (FI-RE51S-HF (JAE) or 187059-51221 (P-TWO))

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	N.C.	No Connection	(2)
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(5)
11	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
12	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
13	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
14	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
15	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	OCLK-	Odd pixel Negative LVDS differential clock input	(5)
18	OCLK+	Odd pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(5)
21	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
22	N.C.	No Connection	(2)
23	N.C.	No Connection	
24	GND	Ground	
25	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(5)
26	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
27	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
28	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
29	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
30	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
31	GND	Ground	
32	ECLK-	Even pixel Negative LVDS differential clock input	(5)
33	ECLK+	Even pixel Positive LVDS differential clock input	
34	GND	Ground	
35	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(5)
36	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
37	N.C.	No Connection	(2)
38	N.C.	No Connection	
39	GND	Ground	
40	N.C.	No Connection	(2)
41	N.C.	No Connection	



42	N.C.	No Connection	(2)
43	N.C.	No Connection	
44	N.C.	No Connection	
45	SELLVDS	LVDS data format selection (2.7V~3.3V→JEIDA, 0V~0.7V/Open→VESA)	(3)(4)
46	N.C.	No Connection	(2)
47	N.C.	No Connection	
48	N.C.	No Connection	
49	N.C.	No Connection	
50	N.C.	No Connection	
51	N.C.	No Connection	

Note (1) LVDS connector pin order defined as follows



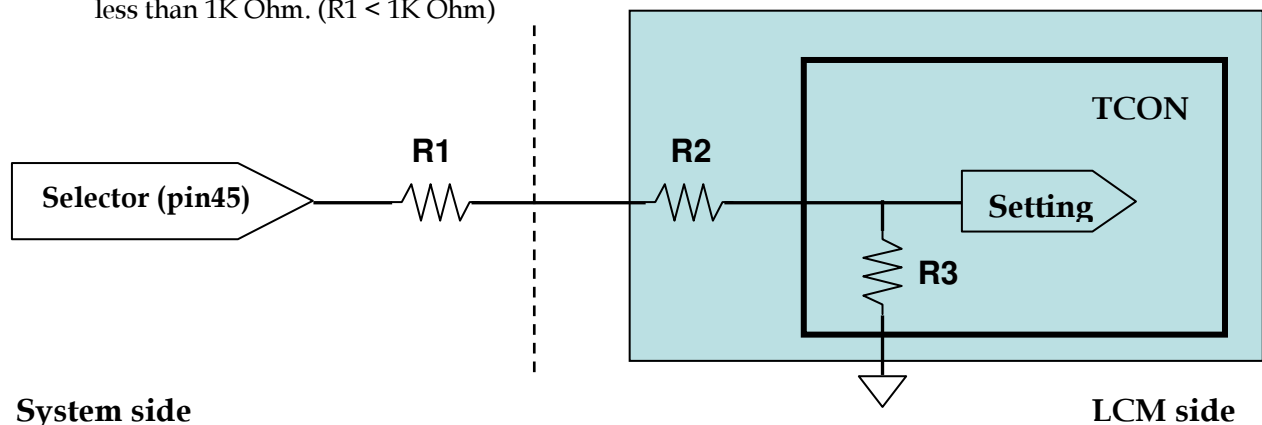
Note (2) Reserved for internal use. Please leave it open.

Note (3) Connect to +3.3V: JEIDA Format, Open or connect to GND: VESA Format.

SELLVDS	Mode
L(default)	VESA
H	JEIDA

L: Connect to GND, H: Connect to +3.3V

Note (4) LVDS signal pin connected to the LCM side has the following diagram. R1 in the system side should be less than 1K Ohm. ( $R1 < 1K \text{ Ohm}$ )



Note (5) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

**5.2 CONVERTER UNIT**

CN1 : S14B-PH-SM4-TB (JST) or CI0114M1HR0-LA (CvilLux)

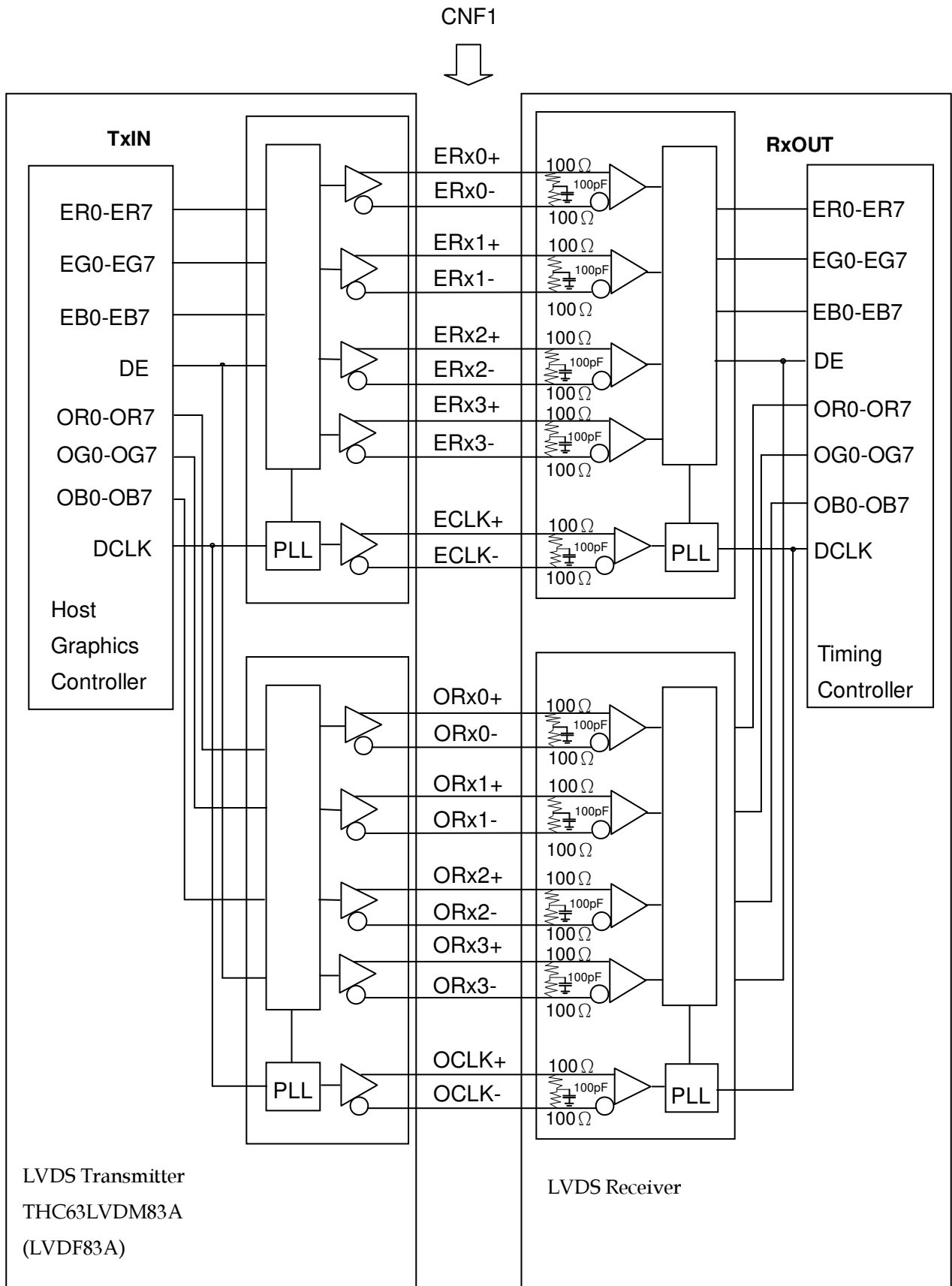
Pin No	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) Abnormal (Open Collector)
12	BLON	BL ON/OFF ON: Hi(2 ~ 5V) OFF: 0~0.8V/ GND
13	NC	NC
14	E_PWM	External PWM Control 5%~100% duty (Open for 100%)

Note (1) If Pin14 is open, E\_PWM is 100% duty.

CN2~CN3 : 51281-1094 (Molex)

Pin No	Symbol	Feature
1	VLED6-	Positive of LED String
2	VLED5-	
3	VLED4-	
4	VLED3-	
5	VLED2-	
6	VLED1-	No Connection
7	NC	
8	NC	Negative of LED String
9	VLED+	
10	VLED+	

5.3 BLOCK DIAGRAM OF INTERFACE



ER0~ER7	Even pixel R data	OR0~OR7	Odd pixel R data
EG0~EG7	Even pixel G data	OG0~OG7	Odd pixel G data
EB0~EB7	Even pixel B data	OB0~OB7	Odd pixel B data
		DE	Data enable signal
		DCLK	Data clock signal

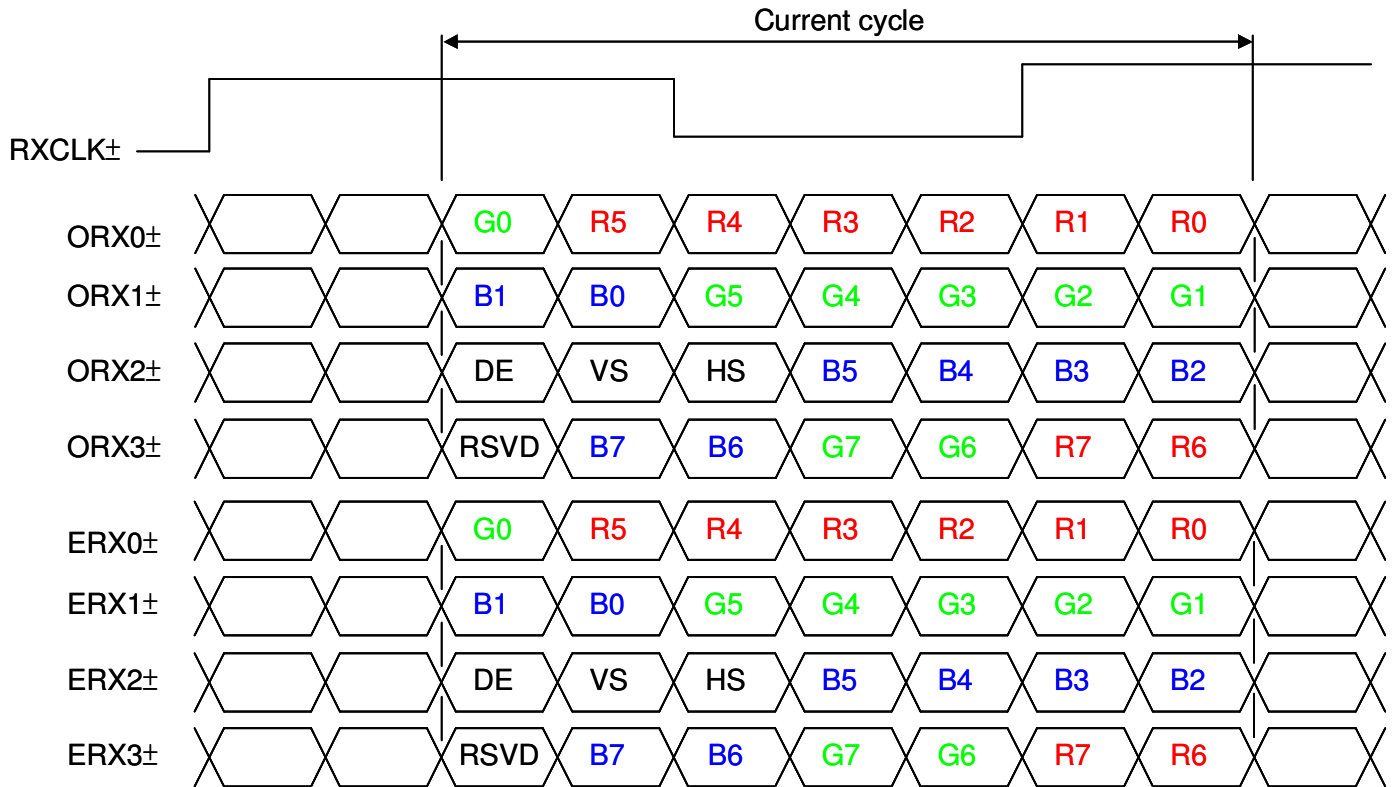
Notes (1) The system must have the transmitter to drive the module.

Notes (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

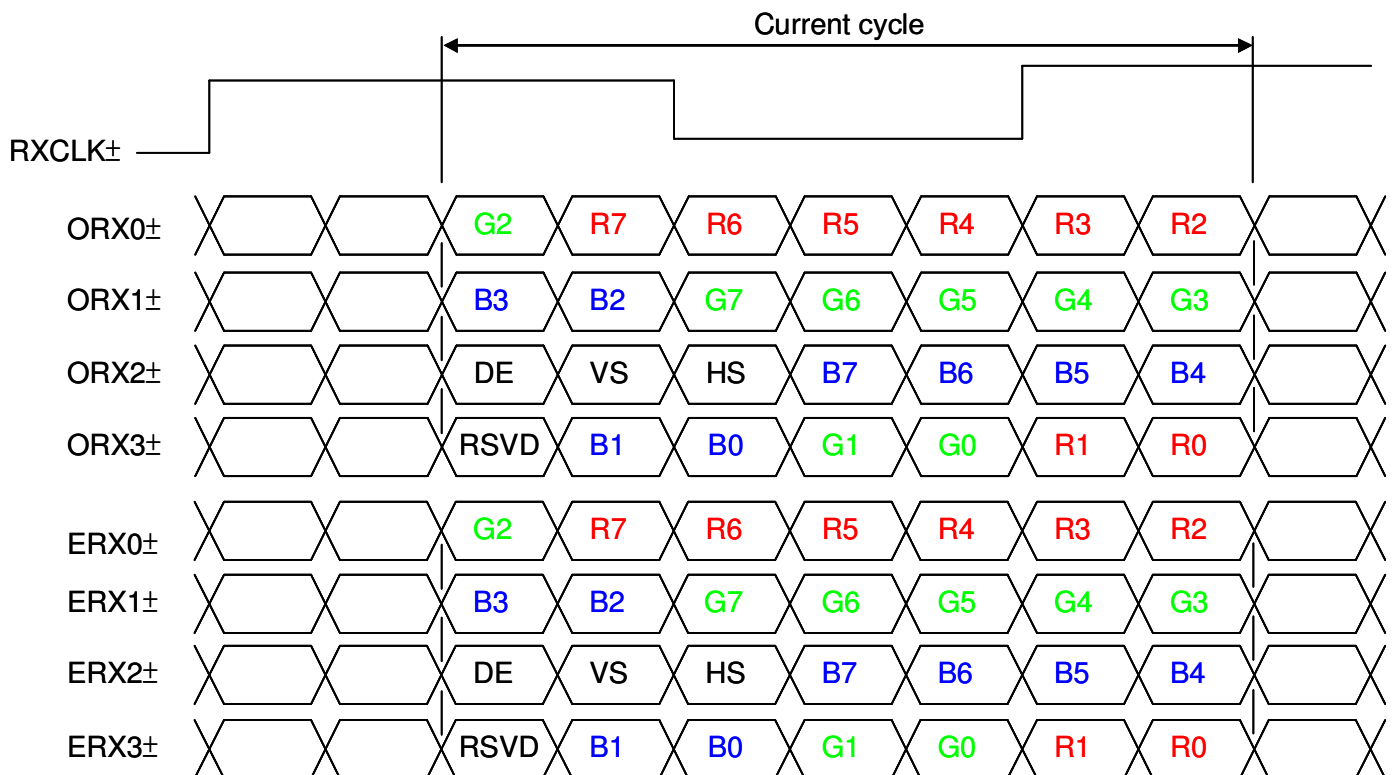
Notes (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

5.4 LVDS INTERFACE

VESA LVDS format : (SELLVDS pin=L/Open)



JEDIA LVDS format : (SELLVDS pin=H)



R0~R7	Pixel R Data (7; MSB, 0; LSB)	DE	Data enable signal
G0~G7	Pixel G Data (7; MSB, 0; LSB)	DCLK	Data clock signal
B0~B7	Pixel B Data (7; MSB, 0; LSB)		

Note (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

**5.5 COLOR DATA INPUT ASSIGNMENT**

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) /Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Gray Scale Of Green	Green (0) /Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0		
Gray Scale Of Blue	Blue (0) /Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	
Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1		

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 °C)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	$F_{clk_{in}}$ (=1/TC)	60	74.25	80	MHz	(1)(5)
	Input cycle to cycle jitter	$T_{rcl}$	—	—	200	ps	(3)
	Spread spectrum modulation range	$F_{clk_{in\_mod}}$	$F_{clk_{in}}-2\%$	—	$F_{clk_{in}}+2\%$	MHz	(4)
	Spread spectrum modulation frequency	$F_{SSM}$	—	—	200	KHz	
LVDS Receiver Data	Setup Time	$T_{lvsu}$	600	—	—	ps	(5)
	Hold Time	$T_{lvhd}$	600	—	—	ps	
Vertical Active Display Term	Frame Rate	$F_{r5}$	47	50	53	Hz	(1)
		$F_{r6}$	57	60	63	Hz	
	Total	$T_v$	1090	1125	1480	Th	$T_v=T_{vd}+T_{vb}$
	Display	$T_{vd}$	1080	1080	1080	Th	(2)
	Blank	$T_{vb}$	10	45	400	Th	(2)
Horizontal Active Display Term	Total	$T_h$	1030	1100	1325	Tc	$T_h=T_{hd}+T_{hb}$
	Display	$T_{hd}$	960	960	960	Tc	(2)
	Blank	$T_{hb}$	70	140	365	Tc	(2)

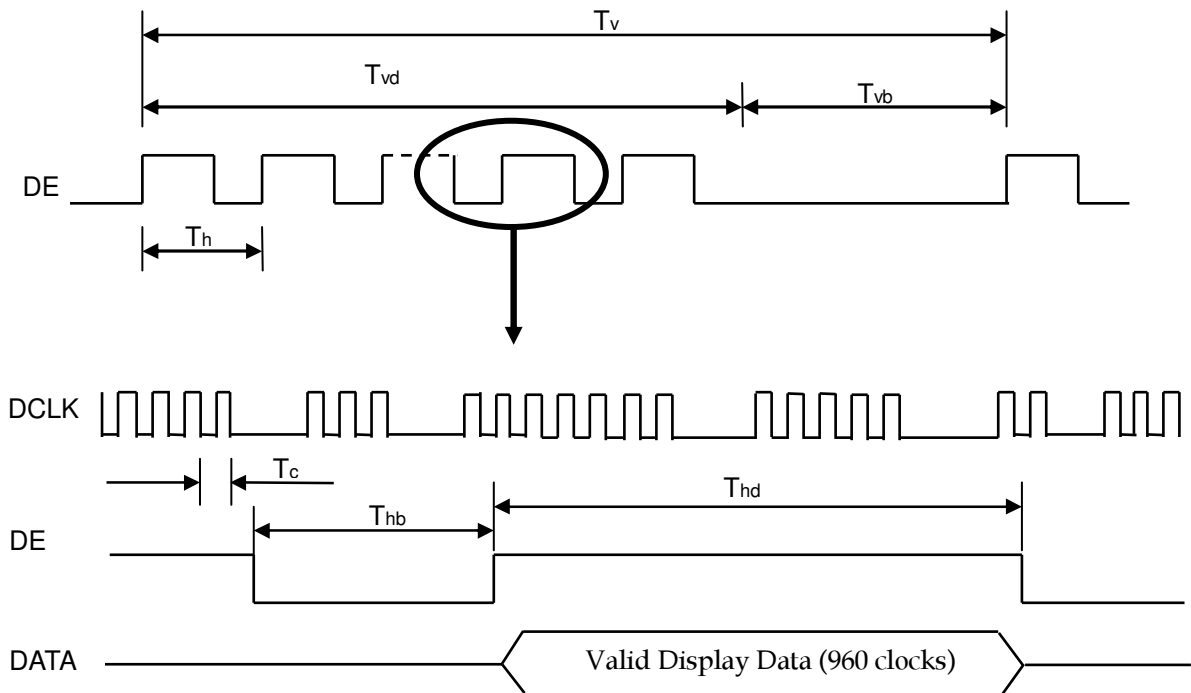
Note (1) Please make sure the range of pixel clock has follow the below equation :

$$F_{clk_{in}(max)} \geq F_{r6} \times T_v \times T_h$$

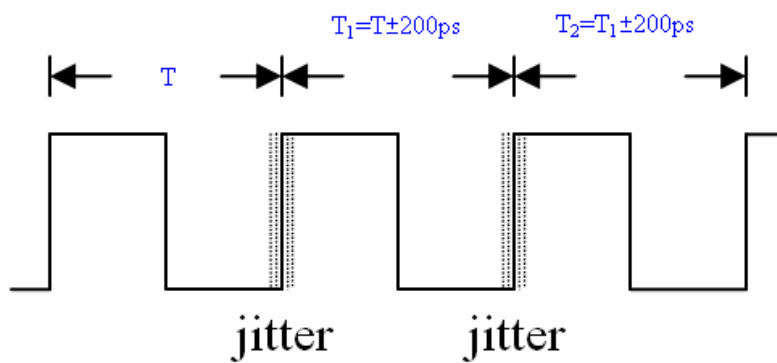
$$F_{r5} \times T_v \times T_h \geq F_{clk_{in}(min)}$$

Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below :

INPUT SIGNAL TIMING DIAGRAM

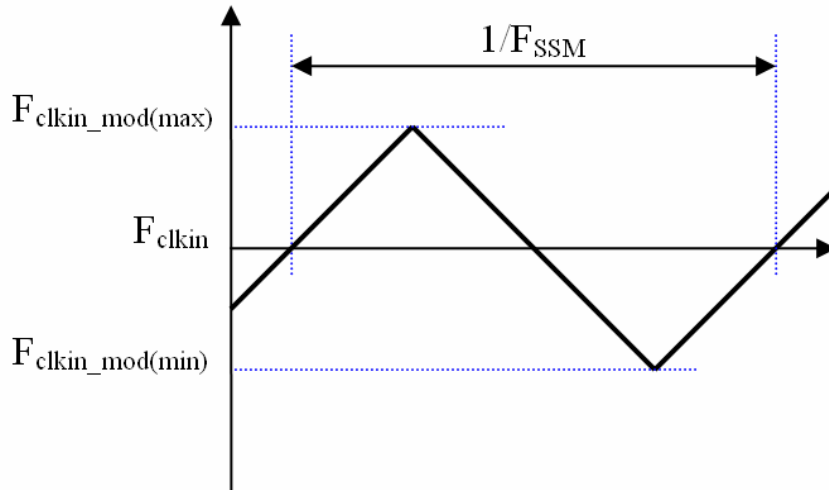


Note (3) The input clock cycle-to-cycle jitter is defined as below figures.  $Trcl = |T_1 - T|$



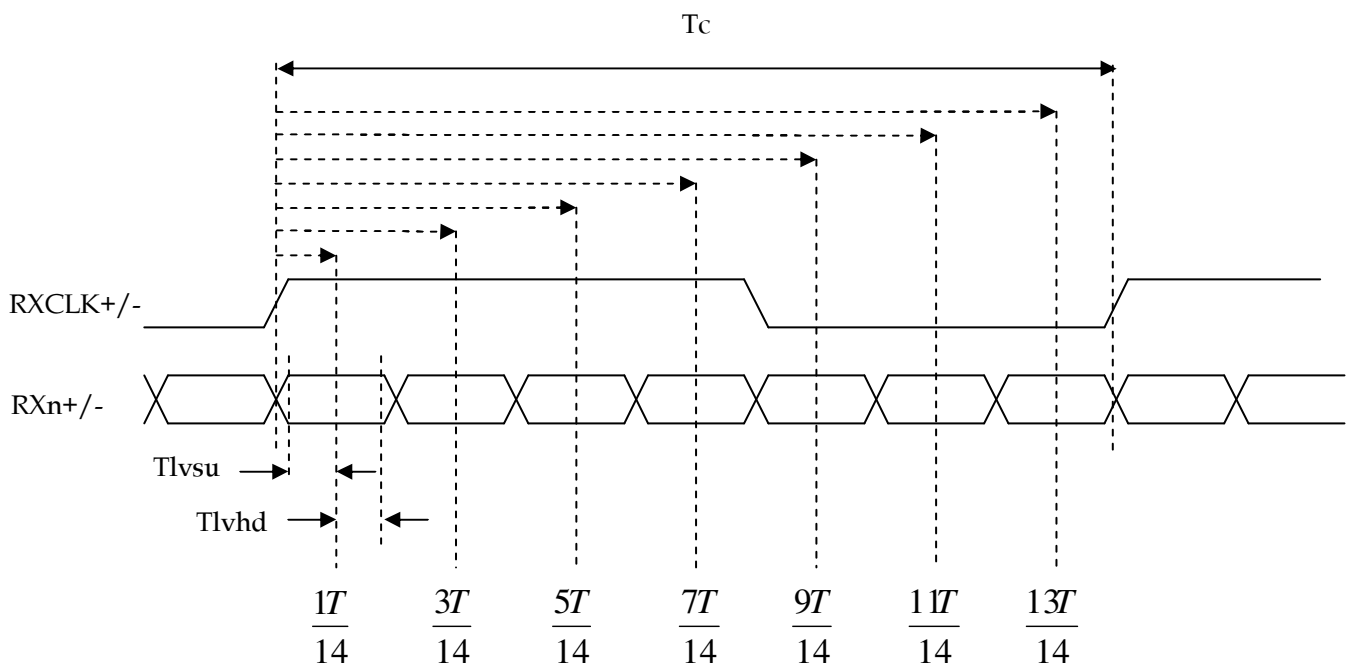
Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.





Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

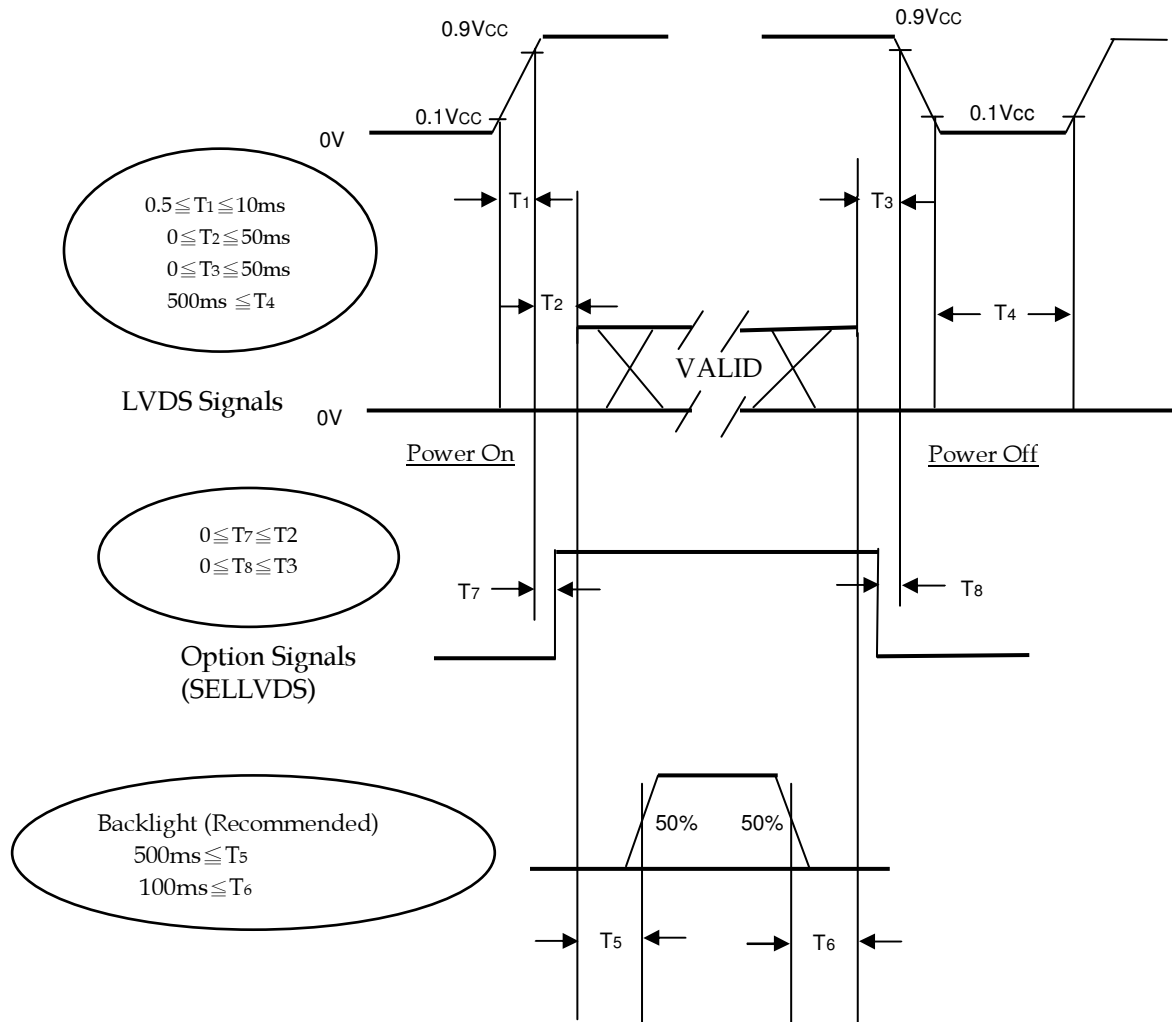
**LVDS RECEIVER INTERFACE TIMING DIAGRAM**



6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 °C)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance. If  $T2 < 0$ , that maybe cause electrical overstress failures.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

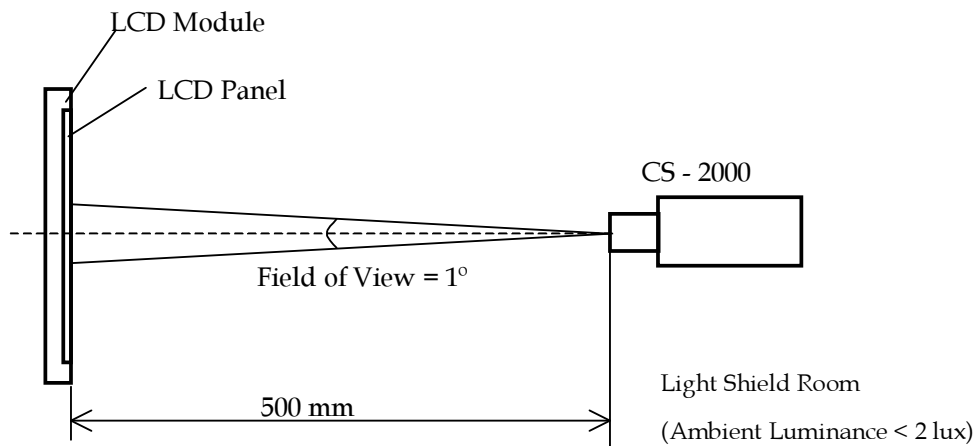
Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	IL	120	mA
Vertical Frame Rate	Fr	60	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



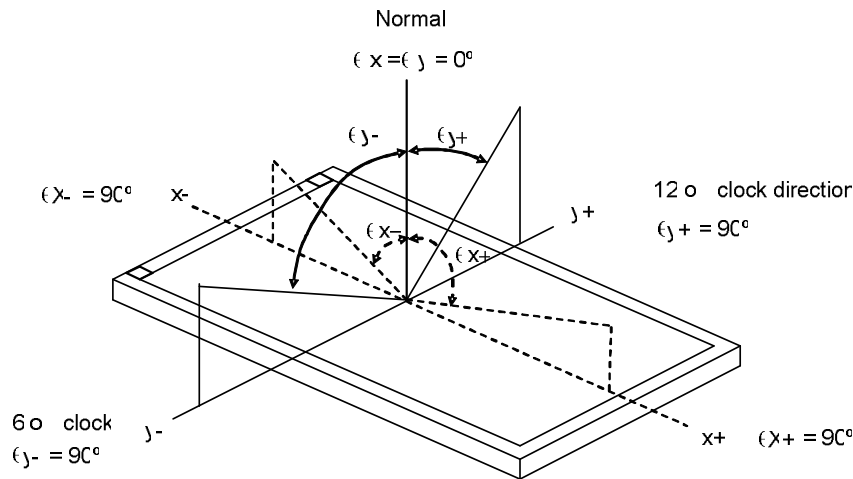
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing angle at normal direction	3500	5000	-	-	Note (2)
Response Time		Gray to gray		-	9.0	18	ms	Note (3)
Center Luminance of White		LC		320	450	-	cd/m <sub>2</sub>	Note (4)
White Variation		$\delta W$		-	-	1.3	-	Note (6)
Cross Talk		CT		-	-	4	%	Note (5)
Color Chromaticity	Red	Rx		Typ. -0.03	Typ. +0.03	0.642	-	-
		Ry	0.331			-		
	Green	Gx	0.290			-		
		Gy	0.612			-		
	Blue	Bx	0.149			-		
		By	0.055			-		
	White	Wx	0.280			-		
		Wy	0.290			-		
	Color Gamut		C.G					72
Viewing Angle	Horizontal	$\theta_{x+}$	CR $\geq$ 20	80	88	-	Deg.	Note (1)
		$\theta_{x-}$						
	Vertical	$\theta_{Y+}$						
		$\theta_{Y-}$						

Note (1) Definition of Viewing Angle ( $\theta_x, \theta_y$ ):

Viewing angles are measured by Autronic Cono-80 (or Eldim EZ-Contrast 160R)



Note (2) Definition of Contrast Ratio (CR) :

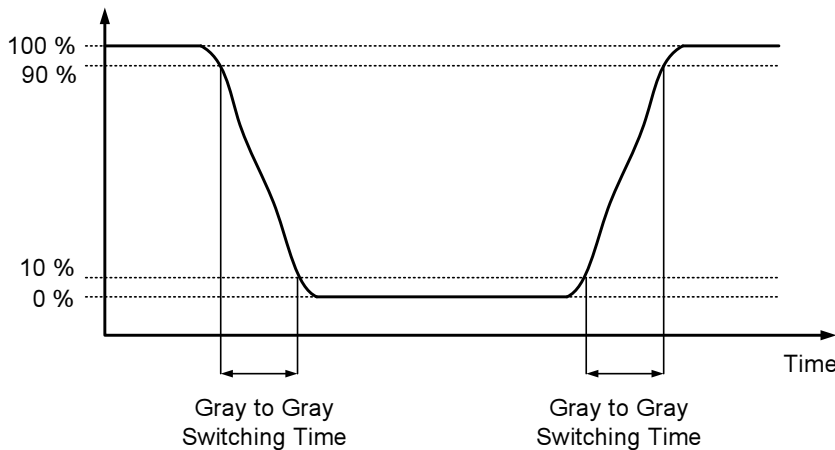
The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time :

**Optical Response**



The driving signal means the signal of gray level 0, 31, 63, 95, 127, 159, 191, 223, 255.

Gray to gray average time means the average switching time of gray level 0, 31, 63, 95, 127, 159, 191, 223, 255. to each other.

Note (4) Definition of Luminance of White ( $L_C, L_{AVE}$ ):

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L (5)$ , where  $L (X)$  is corresponding to the luminance of the point X at the figure in Note (6).

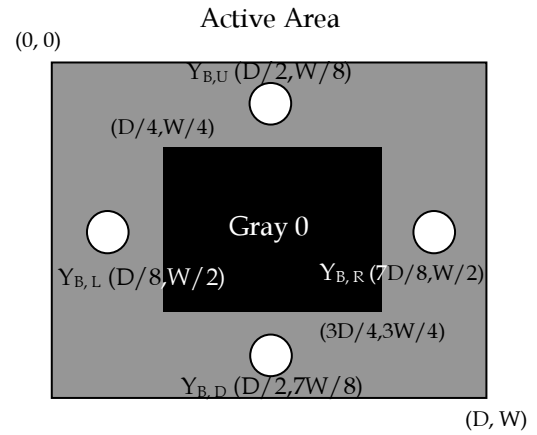
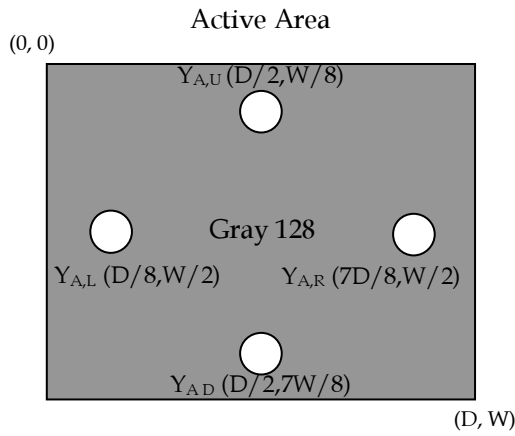
Note (5) Definition of Cross Talk (CT) :

$$CT = | YB - YA | / YA \times 100 (\%)$$

Where :

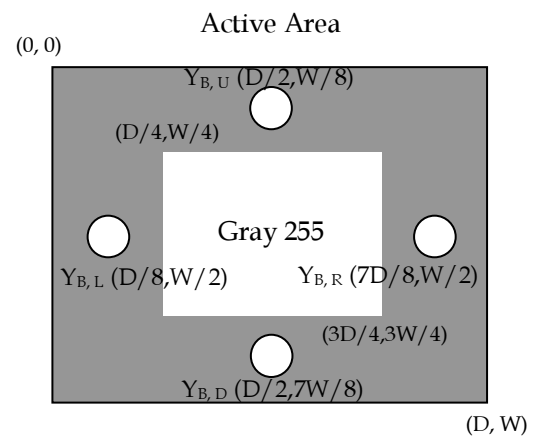
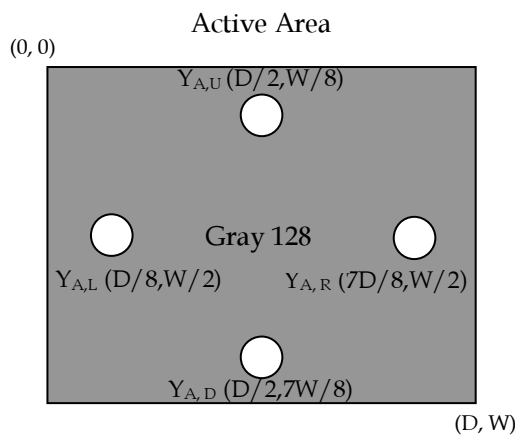
YA = Luminance of measured location without gray level 0 pattern (cd/m<sup>2</sup>)

YB = Luminance of measured location with gray level 0 pattern (cd/m<sup>2</sup>)



YA = Luminance of measured location without gray level 255 pattern (cd/m<sup>2</sup>)

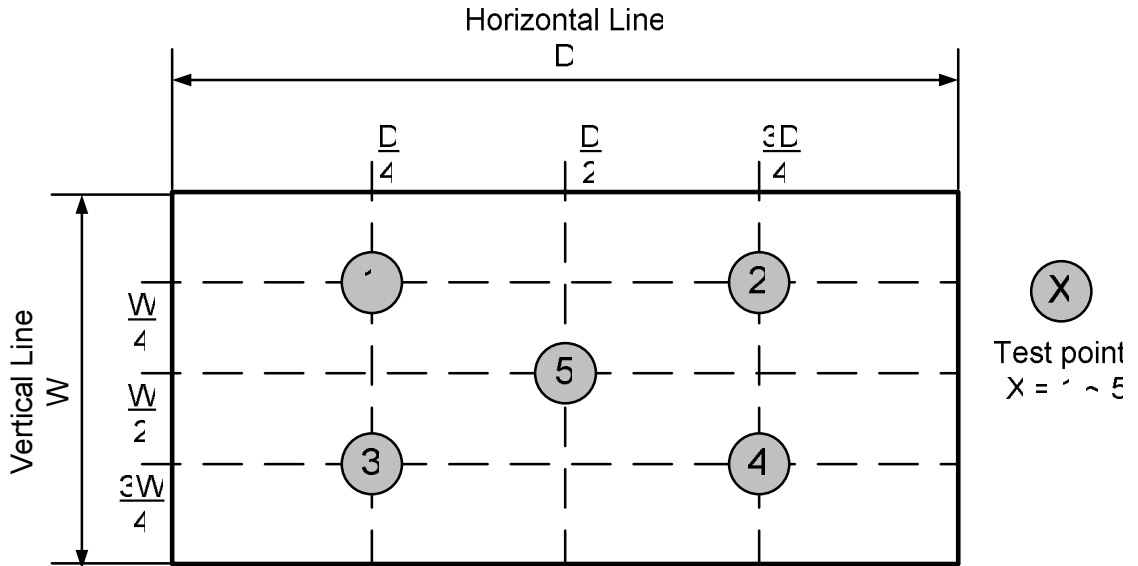
YB = Luminance of measured location with gray level 255 pattern (cd/m<sup>2</sup>)



Note (6) Definition of White Variation ( $\delta W$ ):

Measure the luminance of gray level 255 at 5 points

$$\delta W = \text{Maximum [L (1), L (2), L (3), L (4), L (5)]} / \text{Minimum [L (1), L (2), L (3), L (4), L (5)]}$$



## 8. PRECAUTIONS

### 8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- [ 1 ] Do not apply rough force such as bending or twisting to the module during assembly.
- [ 2 ] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- [ 3 ] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.
- [ 4 ] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- [ 5 ] Do not plug in or pull out the I/F connector while the module is in operation.
- [ 6 ] Do not disassemble the module.
- [ 7 ] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- [ 8 ] Moisture can easily penetrate into LCD module and may cause the damage during operation.
- [ 9 ] When storing modules as spares for a long time, the following precaution is necessary.
  - [ 9.1 ] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
  - [ 9.2 ] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.
- [ 10 ] When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

### 8.2 SAFETY PRECAUTIONS

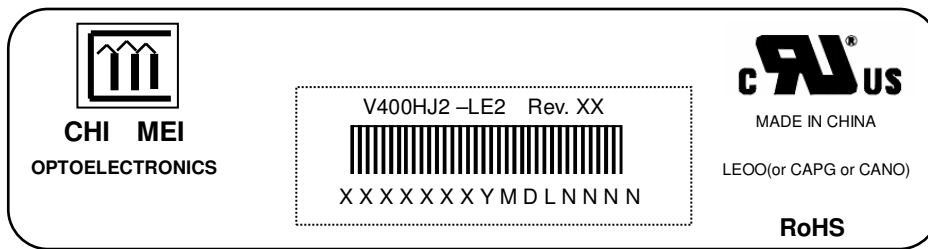
- [ 1 ] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.
- [ 2 ] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- [ 3 ] After the module's end of life, it is not harmful in case of normal operation and storage.



9. DEFINITION OF LABELS

9.1 MODULE LABEL

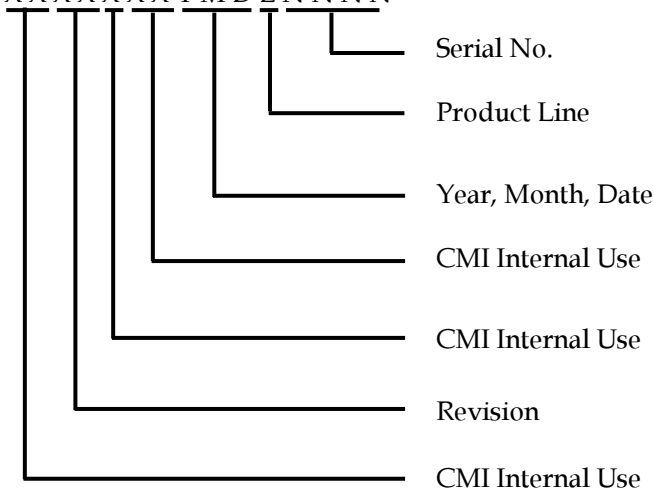
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V400HJ2-LE2

Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.

Serial ID: XXXXXYYMDLNNNN



Serial ID includes the information as below:

Manufactured Date :

Year : 2001=1, 2002=2, 2003=3, 2004=4...2010=0, 2011=1, 2012=2...

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I,O, and U.

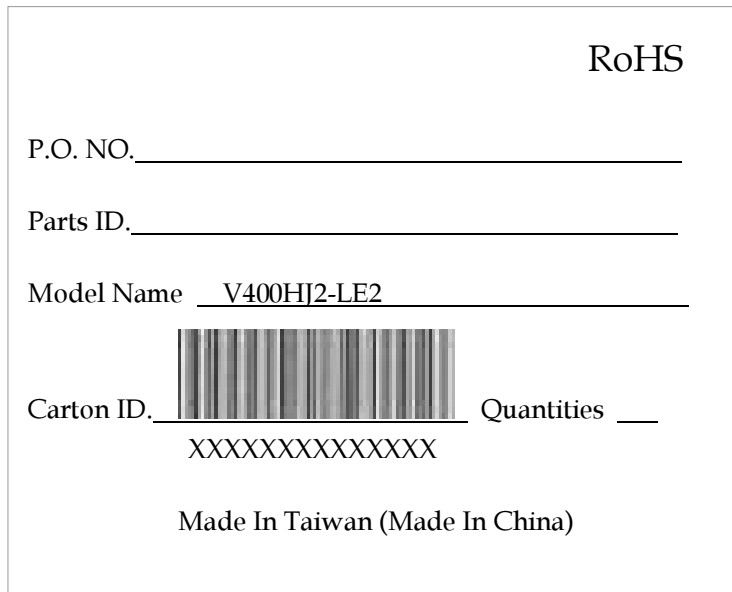
Revision Code : Cover all the change

Serial No. : Manufacturing sequence of product

Product Line : 1 → Line1, 2 → Line 2, ...etc.

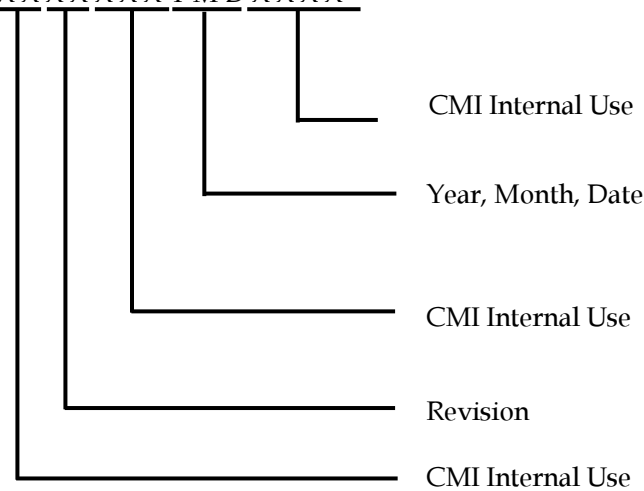
9.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.



(a) Model Name: V400HJ2- LE2

(b) Carton ID:   X X X X X X Y M D X X X X  



Serial ID includes the information as below :

Manufactured Date:

Year: 2010=0, 2011=1, 2012=2...etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I, O, and U.

Revision Code: Cover all the change

(c) Quantities: 5

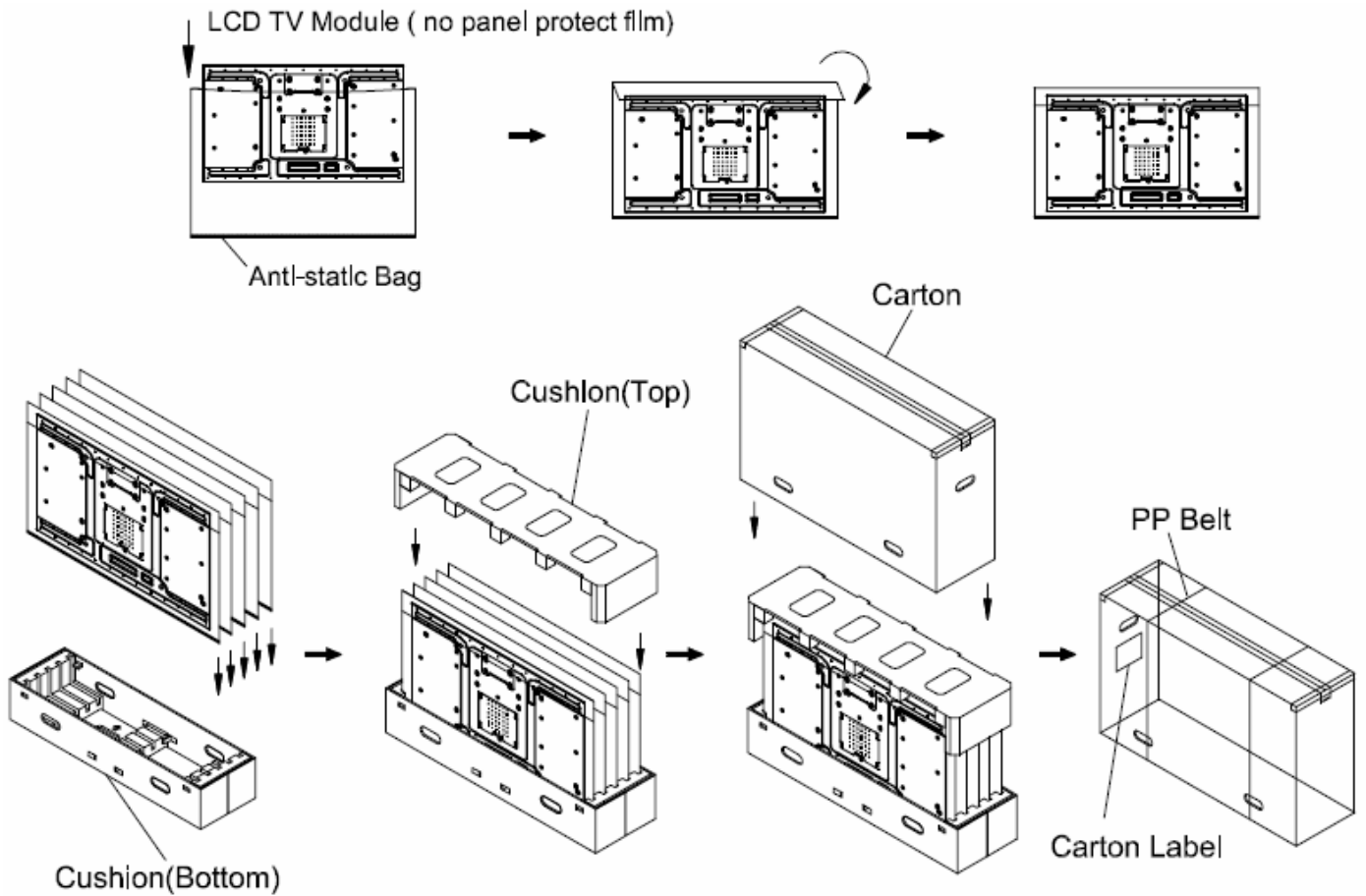
**10. PACKAGING**

**10.1 PACKAGING SPECIFICATIONS**

- (1) 5 LCD TV modules / 1 Box
- (2) Box dimensions : 1035(L)x309(W)x625(H)mm
- (3) Weight : approximately 39 Kg (5 modules per box)

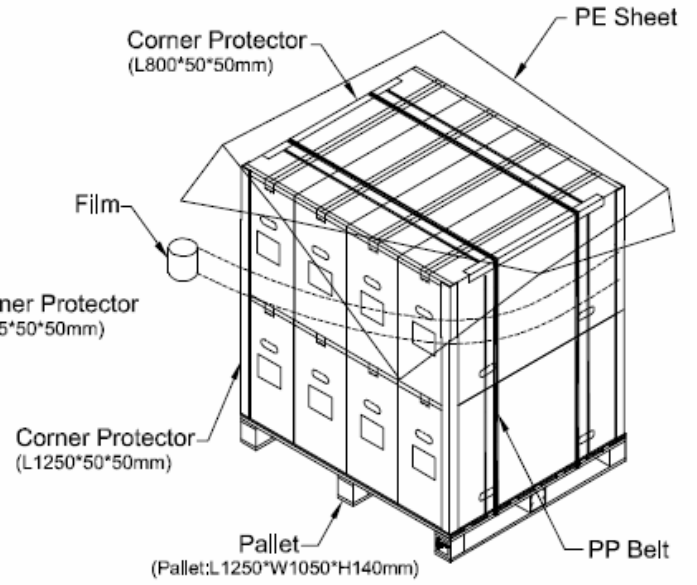
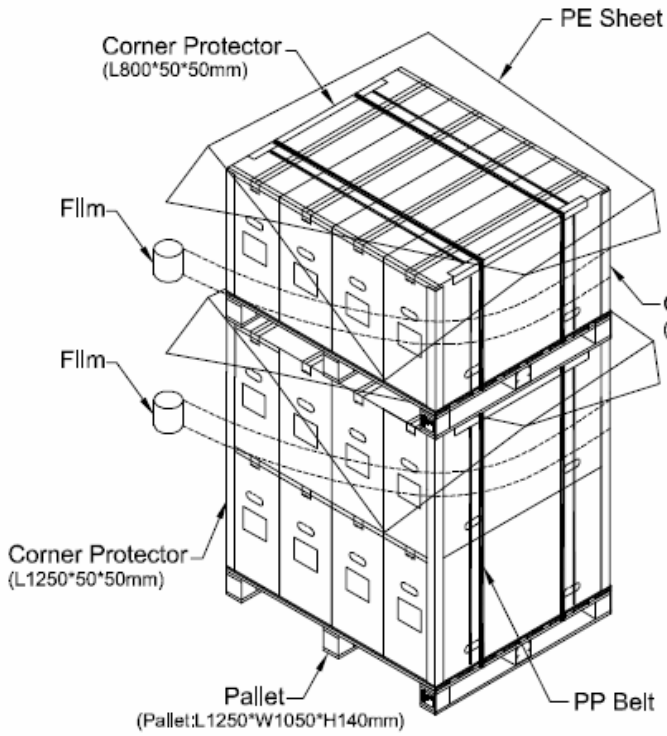
**10.2 PACKAGING METHOD**

Packing method is shown in Figure 10.1 & 10.2

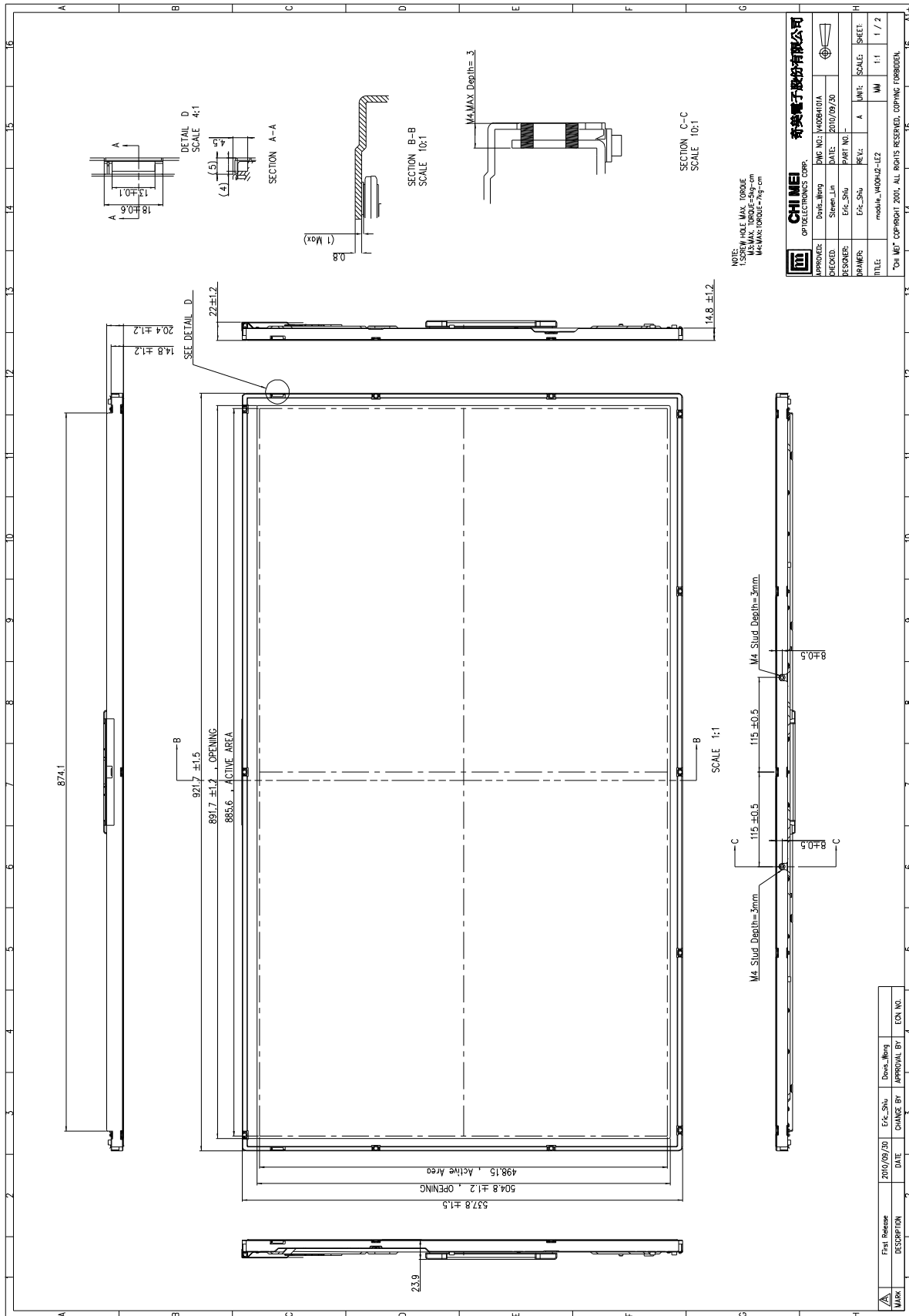


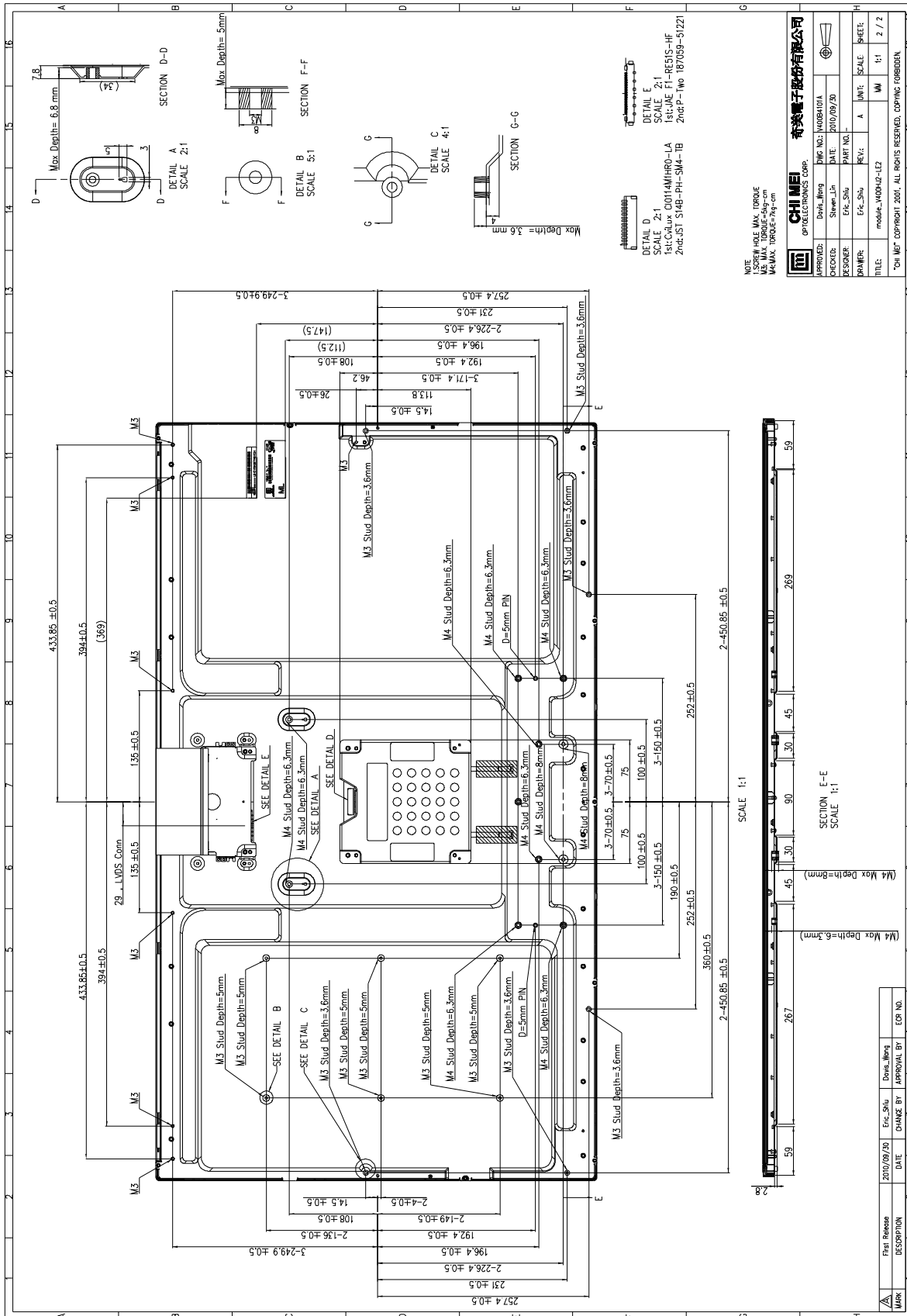
Sea / Land Transportation (40ft Container)

Air Transportation



11. MECHANICAL CHARACTERISTICS





Appendix

	V400HJ2-LE2	V400HJ2-LE2
<b>Product Version</b>	C1	C2
<b>Data IC</b>	Novatek	Himax
<b>Scan IC</b>	Novatek	Himax
<b>TCON</b>	Kawasaki	Faraday
<b>LVDS Connector</b>	JAE	P-TWO